CLAIMS

1. A method for manufacturing electronic semiconductor devices comprising the steps of:

depositing a layer of hydrophobic material on a substrate;

depositing a "deep UV" photo-resist layer on the layer of hydrophobic material;

selectively removing said "deep UV" photo-resist layer in order to form an opening therein and expose a portion of said hydrophobic material;

selectively removing said hydrophobic material in correspondence with the exposed portion thereof in order to expose a portion of said substrate;

etching said substrate in correspondence with said exposed portion thereof through chemical etching with a watery acid solution; and

removing said layer of hydrophobic material and said "deep UV" photo-resist layer from the unexposed portions of the semiconductor substrate.

2. A method according to claim 1, wherein said hydrophobic material is chosen from the group comprising BARC, polytetrafluoroethylene, polyethylene, polystyrene and polyvinyl chloride.

3. A method according to claim 2, wherein said hydrophobic material is BARC.

4. A method according to claim 1, wherein said layer of hydrophobic material has a thickness comprised between 300 Å and 1600 Å.

5. A method according to claim 1, wherein the selective removal of said "deep UV" photo-resist layer is performed through photolithography.

6. A method according to claim 1, wherein the selective removal of said layer of hydrophobic material is performed through plasma etching.

7. A method according to claim 1, wherein the watery solution used in the etching step of said semiconductor substrate comprises hydrofluoric acid with a concentration comprised between 0,1% and 10%.

8. A method according to claim 1, wherein said removing step of the hydrophobic material layer from semiconductor substrate unexposed portions is performed through plasma etching.

9. A method according to claim 1, wherein said removing step of the "deep UV" photo-resist layer from semiconductor substrate unexposed portions is performed through photolithography.

10. A method for manufacturing electronic semiconductor devices, comprising:

depositing a hydrophobic layer directly on a semiconductor layer;

depositing a photo-resist layer on the hydrophobic layer;

selectively removing the photo-resist layer in order to form an opening therein and expose a portion of the hydrophobic layer;

selectively removing the hydrophobic layer in correspondence with the exposed portion thereof to expose a portion of the semiconductor layer;

etching the substrate in correspondence with the exposed portion of the semiconductor layer; and

removing the layer of hydrophobic material and the photo-resist layer from the unexposed portions of the semiconductor layer.

11. The method of claim 10, wherein the hydrophobic layer is chosen from the group comprising BARC, polytetrafluoroethylene, polyethylene, polystyrene and polyvinyl chloride.

12. The method of claim 11 wherein the hydrophobic layer is BARC.

13. The method of claim 10 wherein the hydrophobic layer has a thickness comprised between 300 Å and 1600 Å.

14. The method of claim 10 wherein the photo-resist layer is a "deep UV photo-resist layer.

15. The method of claim 10 wherein selectively removing the hydrophobic layer is performed through plasma etching.

16. The method of claim 10 wherein removing the hydrophobic layer from the unexposed portions of semiconductor layer is performed through plasma etching.

17. The method of claim 10 wherein etching the substrate is performed by chemical etching with a watery acid solution.

18. An intermediate structure for creating an integrated device, comprising:

a semiconductor layer;

a hydrophobic layer positioned directly on the semiconductor layer; and

a photo-resist layer positioned directly on the hydrophobic layer, the photo-resist layer having an opening that exposes a portion of the hydrophobic layer.

19. The intermediate structure of claim 18 wherein the hydrophobic layer has an opening, aligned with the opening in the photo-resist layer, that exposes a portion of the semiconductor layer.

20. The intermediate structure of claim 19, further comprising a semiconductor substrate underlying the semiconductor layer wherein the semiconductor layer has an opening, aligned with the openings in the photo-resist and hydrophobic layers, that exposes a portion of the semiconductor substrate.